Fixed-Point Types in Xilinx Vivado: Example of using the types ufixed and sfixed

Required Files:

To be included in all Vivado projects using the ufixed and sfixed data types:

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd

Specific to this example:

- Fixed_test.vhd
- Fixed_test_tb.vhd

Please note that the files using the fixed-point representation types (in our case, Fixed_test.vhd and Fixed_test_tb.vhd) must contain the following declarations:

library ieee_proposed; use ieee_proposed.fixed_pkg.all;

Step 1:

Create a new project (e.g., sfixed_test) and add

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd, and
- Fixed_test.vhd

to this project as design sources.

PROJECT MANAGER - sfixed_test			
Sources ? _ D 🛙	× Project Summary		
Q ≚ ≑ + 2 ● 0	Overview Dashb	pard	
Design Sources Constraints Simulation Sources isim_1 Design Sources isim_1 Design Sources Hierarchy Libraries Compile Order Properties ? - Compile Order	Settings Edit Project name: Project location: Project location: Project part: Add Sources	sfixed_test C_Users/KrisGaj/Sfixed_test Artix-7 xc7a35tcpg236-1 Add Sources This guides you through the process of adding and creating sources for your project Add or create constraints Add or create design sources Add or create simulation sources	× *
Select an object to see properties	E XILINX.	< Back Next >	Einish Cancel



Step 2:

Add

• Fixed_test_tb.vhd

to the project as a simulation source.





Step 3:

In the Sources window click on the tab Libraries



Step 4:

In the Source File Properties window, set the library name for the files

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd

to

ieee_proposed.

Additionally, change the type of these files to VHDL 2008.



Change the type of Fixed_test.vhd to VHDL 2008. Your Sources window should now look as follows:



Step 5:

Change the type of Fixed_test_tb.vhd to **VHDL 2008**. Your Sources window should now look as follows:



Step 6:

In the Sources window click on the tab Hierarchy.



Step 7:

Run Behavioral Simulation. Display the first 40 ns of the simulation waveforms. You should get waveforms similar to:

Name	Value	0 ns	2 ns	4 ns	6 ns	8 ns	10 ns	12 ns	14 ns	16 ns	18 ns	20 ns	22 ns	24 ns	26 ns	28 ns	30 ns	32 ns	34 r	s :	36 ns	38 ns 40
> ₩A_F[3:-28]	35433480.1		0.0			1865620	54.1875		Ľ		361616	11.375		X		2440153	37.9375			-	35433480	.1875
> ₩B_F[3:-28]	18656264.1		0.0			5243215	5.4375		ΞX		-244007	82.9375		X		4850254	15.5625				18656264	.1875
> VOPCODE[1:0	1.0		0.0								. 0	.5									1.0	
> 😻 S_F[3:-28]	16777216.0		0.0	Ϋ́		710884	19.625		Ϋ́		1176082	28.4375		χ		72904	083.5				167772	16.0
16 clk	1																					
UCLK_PERIOD	10000 ps										100	000 ps										

Step 8:

Highlight in turn, A_F, B_F, and S_F, right-click, and change Real Settings of these signals to: **Fixed point**

Signed

Binary point: 28 (number of binary digits after the dot).

using the following windows:



Name	Value	0 ns	2 ns 4	ns 6ns	8 ns	10 ns 12	2 ns 14 ns	16 ns	18 ns	20 ns	22 ns	24 ns	26 ns	28 ns	30 ns	32 ns	34 r.s	36 ns	38 ns
> ¹ A_F[3:-28]	35433480.1		0.0		1865620	54.1875			361616	11.375				2440153	7.9375			3543348	30.1875
> ₩B_F[3:-28]	18656264.1		0.0		524321	55.4375			-244007	82.9375				4850254	5.5625			1865626	54.1875
> VOPCODE[1:0	1.0		0.0						0	.5								1	.0
> ₩S_F[3:-28]	16777216.0		0.0	_ <u>\</u>	710884	19.625	<u>\</u> _	_	1176082	8.4375	1	ĭ		72904	083.5			16777	216.0
le clk	1																		
UCLK_PERIOD	10000 ps								100	00 ps				1	1				
Real Settings					×														
Please specify how a number value.	nultiple-bit c	object is to	be interpre	eted as a real	4														
• Signed Binary point:	O <u>U</u> nsigned 28	ł)																
Floating point																			
Single pre	ecision																		
Double p	ecision																		
Output Contraction (Contraction)	recision																		
Exponent	width:	1 ‡ F	raction wid	th: 2 🌲	r														
?		ОК	Can	ncel	Apply														

Step 9:

By moving in the simulation window, you should now be able to see timing waveforms for the following operations:

Addition:

Name	Value	0 ns 2 ns 4 n:	s 6 ns 8 ns 10 ns 12 ns	14 ns 16 ns 18 ns 20 ns 22 ns 24 n	ns 26 ns 28 ns 30 ns 32 ns 34 n	s 36 ns 38 ns 40			
> 😻 A_F[3:-28]	2.11199999	0.0	1.11199999973178	2.1554000005126	1.45444500073791	2.111999999973178			
> 😻 B_F[3:-28]	1.11199999	0.0	3.12519999966025	-1.4543999992311	2.89097699895501	1.11199999973178			
> IN OPCODE[1:0	10	00		01		10			
> 😻 S_F[3:-28]	1.0	0.0	4.23719999939203	0.7010000012815	4.34542199969292	1.0			
18 clk	1								
UCLK_PERIOD	10000 ps			10000 ps					

Subtraction:

Name	Value	30 ns	32 ns	34 ns	36 ns	38 ns	40 ns	42 ns	44 ns	46 ns	48 ns	50 ns	52 ns	54 ns	56 ns	58 ns	60 ns	62 ns	64 r.	s é	6 ns	68 ns 70
> 😻 A_F[3:-28]	1.11199999	1.45444	50007379	1	2	.1119999	9973178		X	1	.5676499	9777079		X	3	.1678400	0024199			1.1	973178	
> 😻 B_F[3:-28]	2.23400000	2.89097	69989550	11	1	.1119999	9973178		X	2.76539999991655 1.1457000002265										2.2	110269	
> VOPCODE[1:0	11		01	χ							1	0							11			
> 💖 S_F[3:-28]	2.48420799	4.34542	19996929	2	1.0					-	L.197750	00214577			-	2.022140	0000155			2.4	8420799	896121
18 clk	1																					
UCLK_PERIOD	10000 ps										100	00 ps										

Multiplication:

Name	Value		62 ns	64	s	66 ns	68 ns	70 ns	72 ns	74 ns	76 ns	78 ns	80 ns	82 ns	84 ns	86 1	15 8	8 ns	90 ns	92 ns	94 ns	96 ns	98 ns	100 ns							
> 😻 A_F[3:-28]	3.16784000	3.1	67840000	020			1.111999	9997317	3	X		3.54439	99990820	9	X				2.1	22000001	137091										
> ₩B_F[3:-28]	1.14570000	1.1	45700000	020			2.234000	0011026	ə'	×χ		1.34430	00018596	6	X				3.2	32220001	.51873			s 100 n:							
> VOPCODE[1:0	10		10										11								Żχ		00								
> 😻 S_F[3:-28]	2.02214000	2.0	22140000	00		2	2.484207	9989612:	1	÷χ	4.76473692432046						6.	858770	84732056	5	Ťχ		0.0								
16 clk	0																														
18 CLK_PERIOD	10000 ps												10000	ps																	