

Fixed-Point Types in Xilinx Vivado: Example of using the types ufixed and sfixed

Required Files:

To be included in all Vivado projects using the ufixed and sfixed data types:

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd

Specific to this example:

- Fixed_test.vhd
- Fixed_test_tb.vhd

Please note that the files using the fixed-point representation types (in our case, Fixed_test.vhd and Fixed_test_tb.vhd) must contain the following declarations:

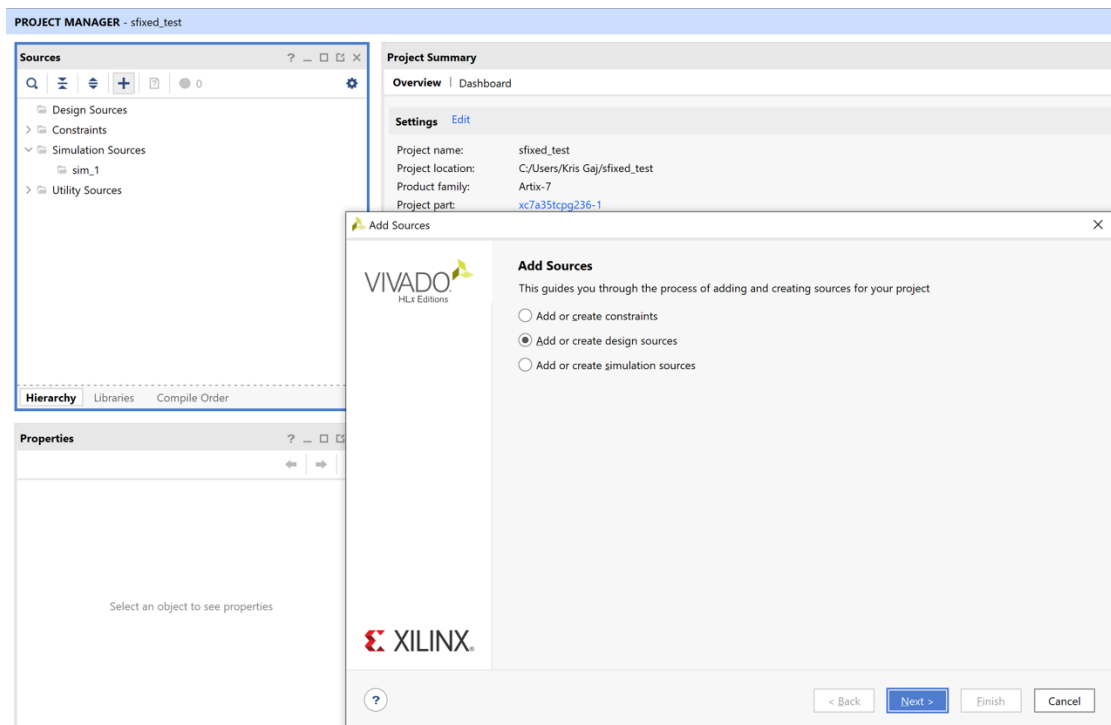
```
library ieee_proposed;  
use ieee_proposed.fixed_pkg.all;
```

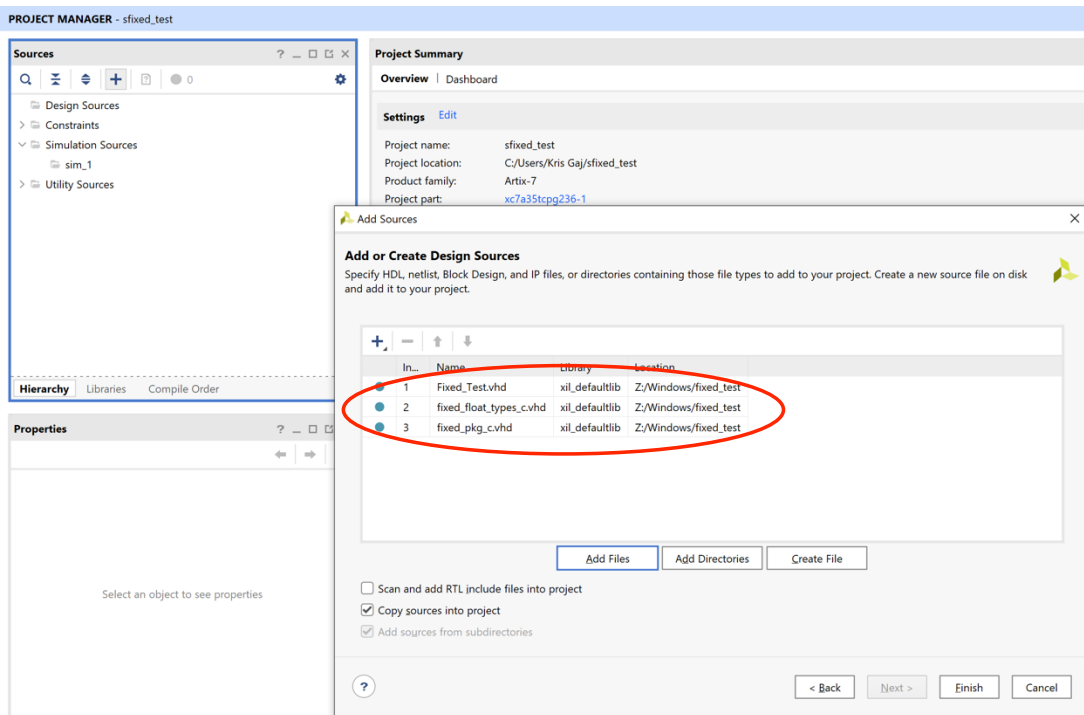
Step 1:

Create a new project (e.g., sfixed_test) and add

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd, and
- Fixed_test.vhd

to this project as design sources.

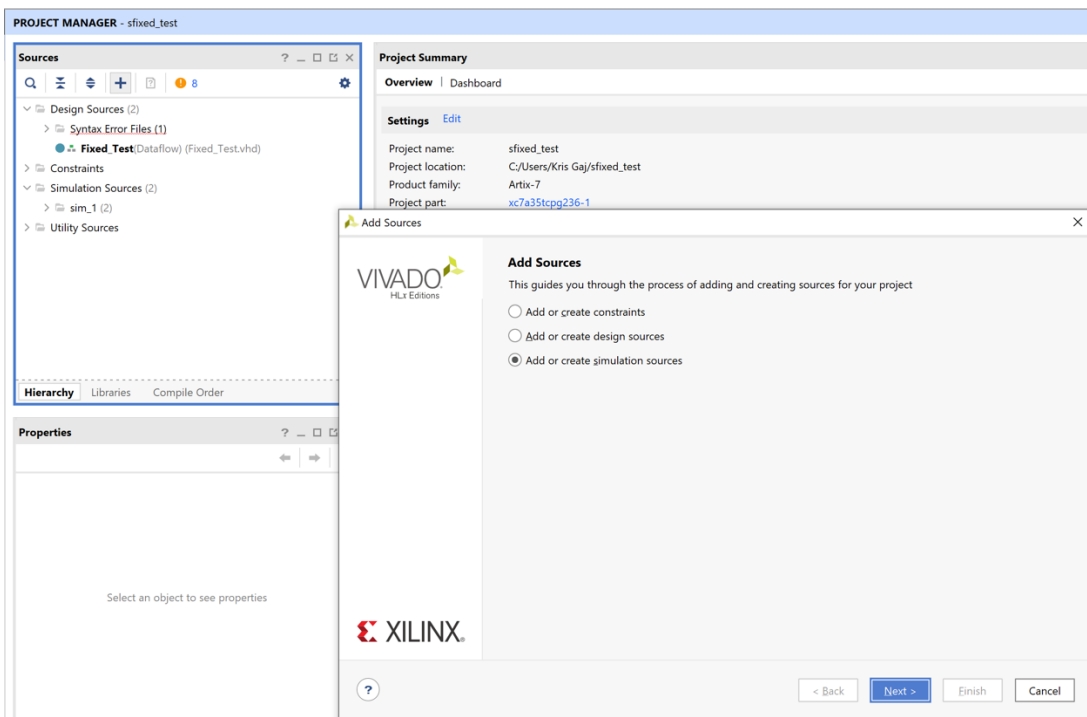


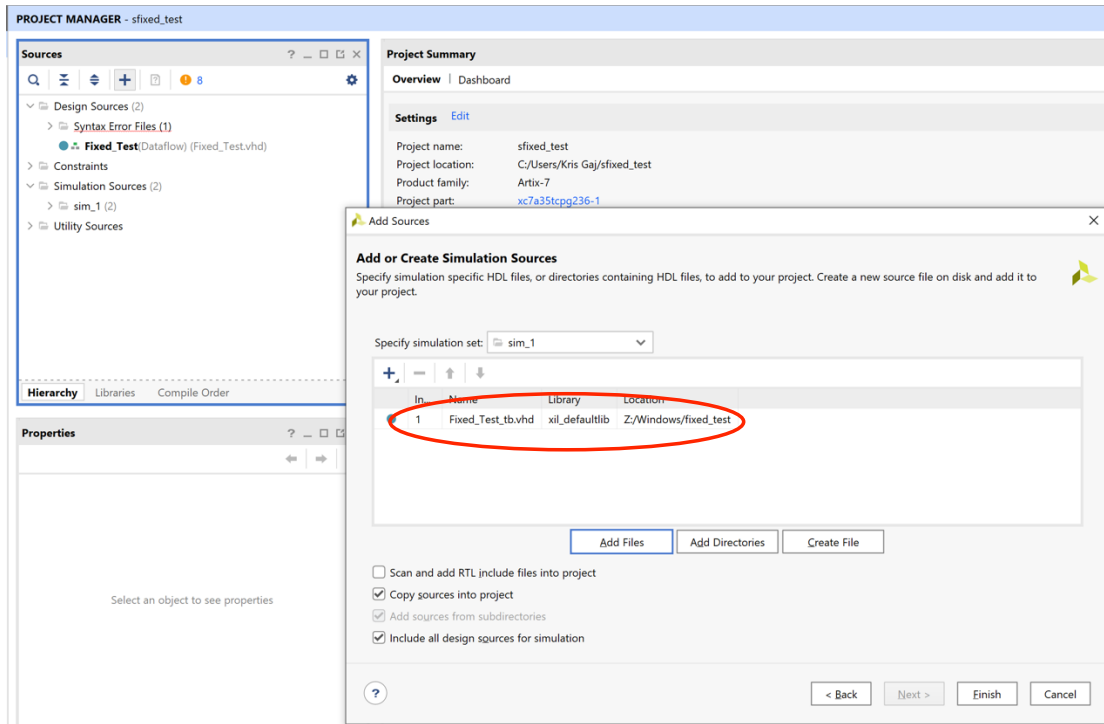


Step 2:

Add

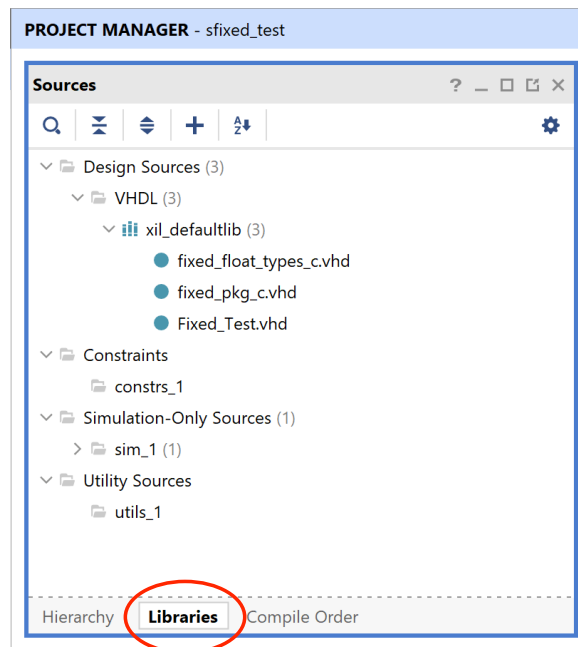
- Fixed_test_tb.vhd to the project as a simulation source.





Step 3:

In the Sources window click on the tab **Libraries**



Step 4:

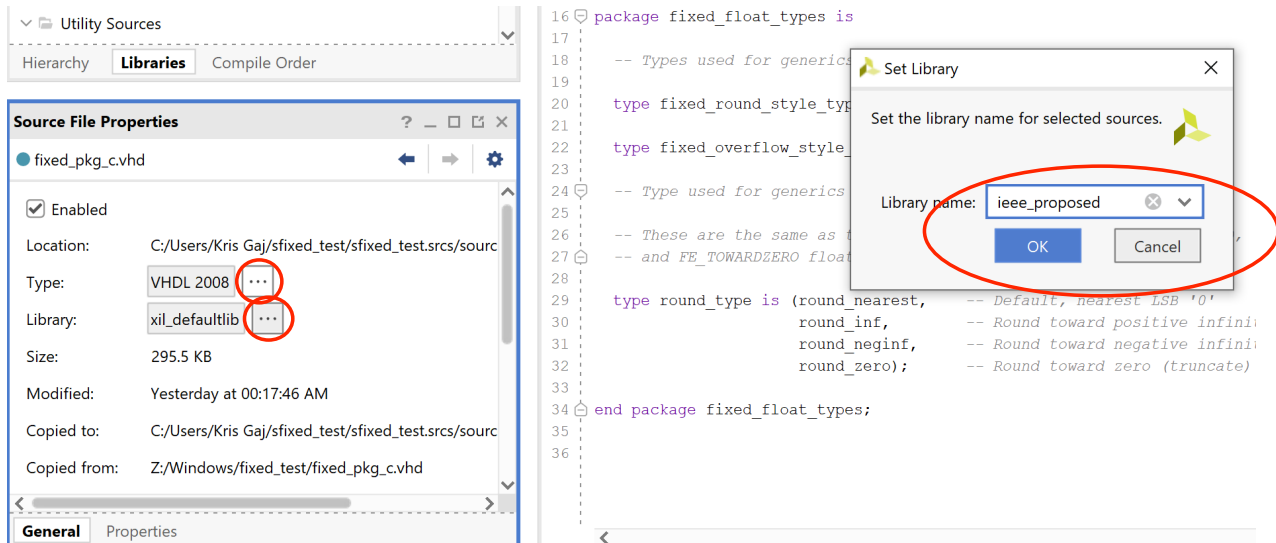
In the Source File Properties window, set the library name for the files

- fixed_float_types_c.vhd
- fixed_pkg_c.vhd

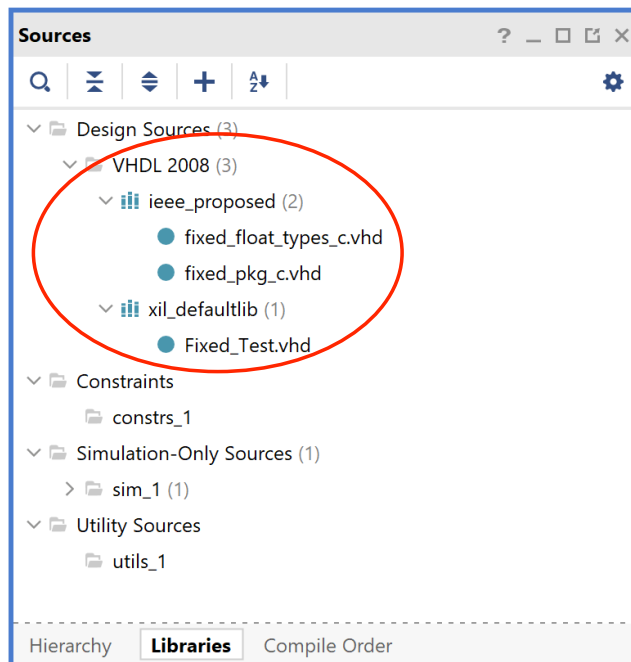
to

ieee_proposed.

Additionally, change the type of these files to **VHDL 2008.**

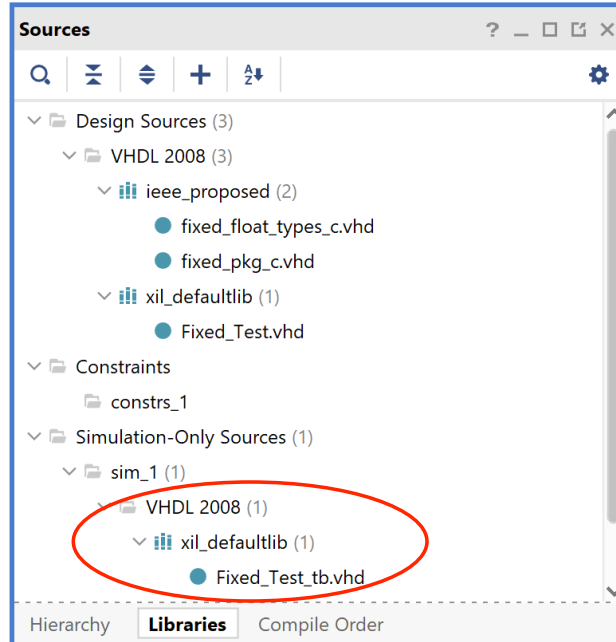


Change the type of Fixed_test.vhd to **VHDL 2008.** Your Sources window should now look as follows:



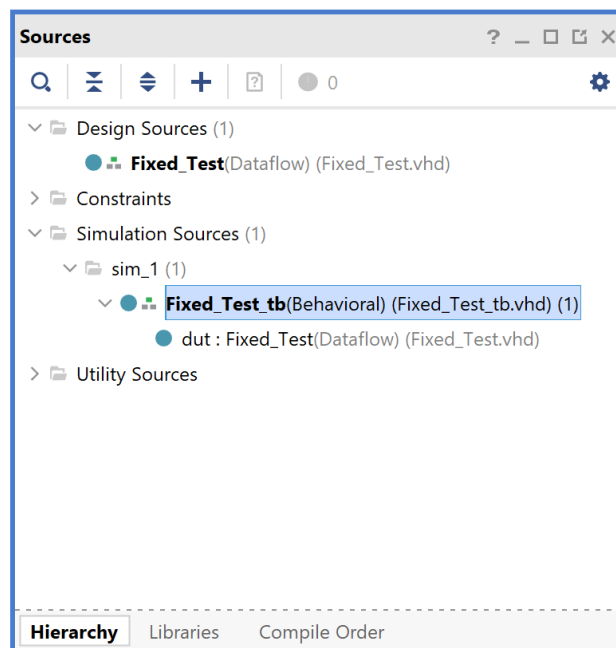
Step 5:

Change the type of Fixed_test_tb.vhd to **VHDL 2008**. Your Sources window should now look as follows:



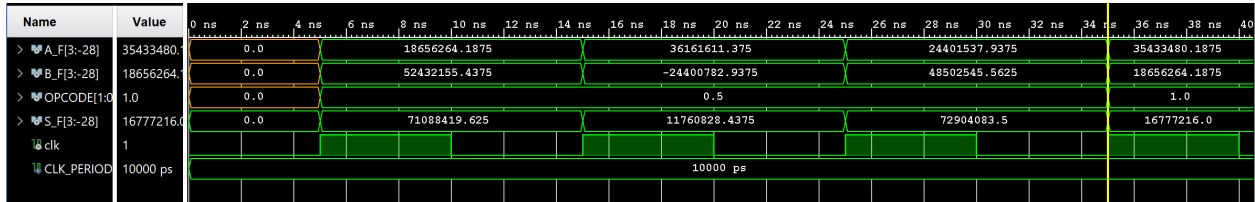
Step 6:

In the Sources window click on the tab **Hierarchy**.



Step 7:

Run Behavioral Simulation. Display the first 40 ns of the simulation waveforms. You should get waveforms similar to:



Step 8:

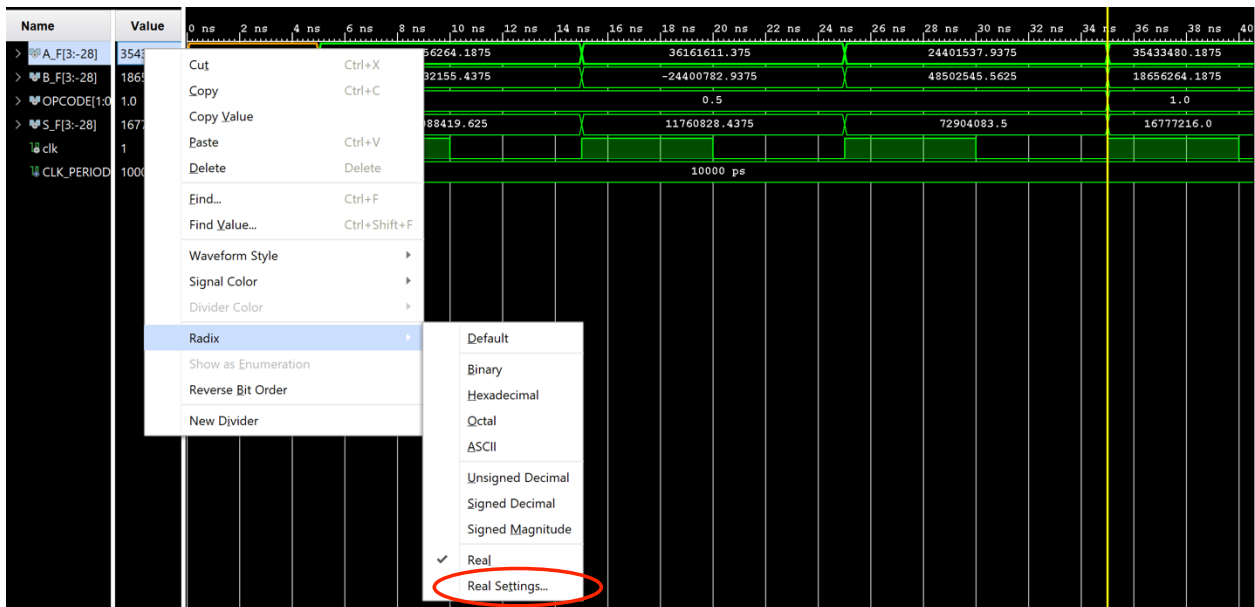
Highlight in turn, A_F, B_F, and S_F, right-click, and change Real Settings of these signals to:

Fixed point

Signed

Binary point: 28 (number of binary digits after the dot).

using the following windows:



Multiplication:

